REMARKS/ARGUMENTS

Objection to the Specification

The specification has been objected to by the Examiner. In particular, the abstract is objected to because it exceeds 150 words. Applicants have amended the abstract to be less than 150 words. As such, Applicants respectfully submit that objection to the specification is traversed.

Rejection under 35 USC § 112

Claims 2-26 stand rejected under USC § 112 as failing to comply with the enablement requirement. In particularly, the Examiner states that it is un-enabling for forming a barrier stack to comprise elements which do not function as a barrier layer such as capacitor structure and plug. Claims 9-12, 14, 16-18, 20-22 and 25-26 have been cancelled without prejudice. As such, the rejection to these claims is moot. Applicants have amended claim 2 to recite a barrier stack which serves as a barrier layer for a capacitor over plug structure. Forming conventional capacitor over plug structures are well known in the art. See, for example, Wang et al. Applicants therefore submit that this basis for rejecting the claims is overcome and respectfully request its withdrawal.

Rejection under 35 USC § 102

Claims 1-26 are rejected by the Examiner under 35 USC § 102(e) as being anticipated by US Patent 6,339,007 (Wang et al). Claims 9-12, 14, 16-18, 20-22 and 25-26 have been cancelled without prejudice. As such, the rejection to these claims is moot. As for the 1-8, 13, 15, 19 and 23-24, Applicants respectfully disagree.

Wang et al. describes a ferroelectric capacitor over a plug. The barrier layer comprising TiN, TaN, TiAlN, TaAlN or TaSiN is located above the plug and bottom capacitor electrode. The barrier layer is formed by chemical vapor deposition or reactive sputtering. See Wang et al., col. 3 at lines 26-33. A bottom electrode is located above the barrier layer. The bottom electrode comprises first and second electrode layers. The electrode layers are deposited by sputtering. The first electrode layer can include a bottom Ir

layer and a top IrO_2 layer. The grain boundaries of the bottom and top layers of the first electrode layer are mismatched. See Wang et al., col. 3 at lines 46-56, col. 6 at lines 53-65 and Fig. 16.

In contrast, claim 1 recites a barrier stack having first and second barrier layers with mismatched grain boundaries separated by a thin intermediate layer. The intermediate layer is formed by a thermal process in an oxidizing ambient (e.g., annealing or thermal or rapid thermal oxidation) to stuff the grain boundaries on or near the top surface of the first barrier layer. The stuffed grain boundaries and mismatched grain boundaries of the first and second barrier layers enhance the barrier properties of the barrier stack.

Applicants submit that forming a barrier stack with an intermediate layer formed from a thermal process between first and second barrier layers to stuff the grain boundaries on or near the top surface of the first barrier layer is nowhere taught or suggested by Wang et al. Wang et al. only teaches or suggests forming a barrier layer using reactive sputtering or chemical vapor deposition. Even if the first electrode layer of Wang et al. were assumed to be a barrier stack, it still fails to teach or suggest the invention as recited in claim 1. In particular, Wang only teaches forming the top and bottom layers of Ir and IrO_2 by sputtering. There is no mention of forming an intermediate layer by a thermal process between the top and bottom layers to stuff the grain boundaries on or near the top surface of the bottom layer. Applicants therefore submit Claim 1, as amended, is patentable over Wang et al. Since claims 2-8, 13, 15, 19 and 23-24 are directly or indirectly dependent on claim 1, these claims are also patentable.

With respect to newly added claims 27, 37, and 46, these claims recite a capacitor over plug structure, a method for forming a capacitor over plug structure or a method of forming a barrier stack which includes a barrier stack. Like claim 1, the barrier stack includes a first barrier layer, an intermediate layer formed by a thermal process in an oxidizing ambient to stuff the grain boundaries on or near the top surface of the first barrier layer and a second barrier layer on the intermediate layer, wherein the first and second barrier layers have mismatched grain boundaries. As already discussed, these claim features are nowhere taught or suggested by Wang et al. Therefore, Applicants submit that these claims are patentable over Wang et al. Since newly added claims 28-36, 38-45 and 47-56 are dependent directly or indirectly on claims 27, 37 or 46, these claims are also patentable over Wang et al.

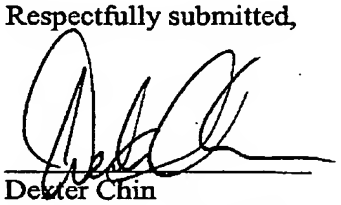
Conclusion

In view of the foregoing, Applicants believe that all claims now pending in this application are in condition for allowance. The issuance of a formal Notice of Allowance at an early date is respectfully requested.

Should the Examiner believe that a telephone conference would expedite prosecution of this application, please telephone the undersigned attorney at his number set out below.

Date: Oct 09, 2003

Respectfully submitted,



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